REMARKS

Reconsideration and allowance of this application, as amended, is respectfully requested.

This amendment is in response to the Office Action dated April 23, 2003.

By the present amendment, the specification has been amended to correct the minor informality noted in paragraph 5 of the Office Action. The drawings are also amended to respond to the objection to the drawing set forth in paragraph 4 of page 2 of the Office Action. In addition, claim 7 has been amended to respond to the 35 U.S.C. § 112, second paragraph, rejection set forth in the Office Action. By virtue of these amendments, reconsideration and removal of the objection to the drawings, the objection to the specification and the 35 U.S.C. § 112, second paragraph, rejection is respectfully requested.

Also by the present amendment, independent claims 1 and 2 have been amended, together with the amending of claim 4, to clarify the invention. Non-elected claims 9-20 have been cancelled, without prejudice to the Applicants' right to file a Divisional application directed to these claims. In addition, new claims 21-35 have been added to define further features of the present invention, as well be discussed below.

Briefly, the present invention is directed to an improved semiconductor device of the type in which a gate insulating film is used in a field effect transistor which has a higher dielectric constant than that of a silicon dioxide film. In particular, the present invention is directed to such a semiconductor device which overcomes problems noted by the inventor in cases where a gate electrode is disposed to overlap the source and drain region of the field effect transistor in a plan configuration.

As discussed in the Background of the Invention, for example, beginning on page 2, line 18 et seq., the use of an insulating film having a high dielectric constant is effective for reducing film thickness to a greater degree than is possible with silicon dioxide film. However, as discussed on page 3, line 9 et seq. of the specification, the use of such high dielectric constant material for gate insulating film can also lead to deterioration of the element characteristics due to an increase in a gate electric field leading to current leakage. In the past, as discussed on page 3, line 16 et seq. of the specification, steps have been taken to reduce this problem by forming the gate insulating film to be shorter in length in the gate length direction than the gate electrode. However, as discussed beginning on page 4, line 7 et seq. of the specification, prior arrangements using such a structure with the overlapping gate electrode have not accounted for two problems which can arise in such structures.

The first of these problems is discussed, for example, on page 4, line 9 et seq. Specifically, because such high dielectric constant insulating films typically use metal oxides, the metal from the high dielectric constant gate insulating film is undesirably introduced into the silicon substrate. This leads to increased leakage current, thereby deteriorating the element characteristics of the device.

In addition, as discussed on page 4, line 22 et seq., when a high dielectric constant insulating film is used as the gate insulating film, the device characteristics are likely to be reduced by a fringe effect due to the increase of capacitance (referred to as fringe capacitance) between the overlapping gate edge and the source and drain regions of the field effect transistor. Accordingly, the present invention is directed to reducing the undesirable effects of both of the above-noted phenomena.

For the Examiner's convenience in reviewing this matter, a sketch is provided which is an enlarged and marked copy of a portion of Fig. 2A of the present application. As can be seen in the attached sketch and in Fig. 2A of the application, the gate insulating film formed of high dielectric constant material 103 is located under the gate electrode 4, with both the gate electrode and the high dielectric constant insulating film extending over the source and drain regions formed in the substrate. In particular, an upper end portion A of the gate insulating film 103 is located inwardly of the edge portion of the gate electrode 104 and also to be over the source and drain region of the transistor. As can be appreciated from the attached sketch, by forming the upper end portion A for the high dielectric constant insulating material 103 in this manner, a gap is provided under the overhanging gate electrode 104 and the thickness of the high dielectric constant insulating film 103 is gradually decreased in thickness toward a lower end portion of the gate insulating film that is actually located outwardly in a gate length direction from the end portion of the gate electrode 104. The upper end portion A of the high dielectric constant insulating film 103 is located to be within a region B in which the gate electrode 104 overhangs the source and drain regions.

In conjunction with the structure of the high dielectric constant insulating film 103, as discussed on page 9, line 3 et seq., a lower dielectric constant insulating film 106 (such as silicon dioxide) can be formed over the tapered end portion of the high dielectric constant insulating film 103 in the area under the gate electrode 104 and between the upper and lower end portions of the gate insulating film 103. The benefits of this are discussed on page 16, line 6-17 as follows:

> "With this semiconductor device, if the insulating film having a high dielectric constant is present on the region in which the channel region and the source and drain regions continuous with the channel region overlap with the gate electrode, it is possible to increase the

> amount of induced charge flowing through the channel region. On the other hand, a high electric field occurs between the gate edges and the source and the drain. Therefore, such a configuration has been adopted that an insulating film having a relatively low dielectric constant such as a silicon dioxide film is disposed at this site. This configuration is effective for reducing the fringe capacitance."

In other words, by virtue of the structure illustrated in Fig. 2A and the attached sketch, it is possible to take advantage of using a high dielectric constant gate insulating film such as 103 under a gate electrode 104 which overhangs the source and drain regions while overcoming the disadvantages of introducing undesirable metal material into the source and drain regions of the silicon substrate and undesirable fringe capacitance.

Reconsideration and removal of the rejection of claims 1, 2, 3, 5 and 7 over U.S. Patent 6,495,890 to Ono is respectfully requested. In the Office Action, a reference is made to Fig. 5G of Ono as reading on the claim language set forth in the originally presented claims. Specifically, the gate insulating film 111 of Ono with its recessed side surfaces is equated to the claimed structure.

By the present amendment, it is respectfully submitted that the distinctions of the present invention over the structure of Ono are clearly defined. In the presently amended independent claims 1 and 2, the arrangement shown in Fig. 2A and the attached sketch of the upper end portions of the gate insulating film being positioned inwardly from both end portions of the gate electrode and lower end portions of the gate insulating film. As such, the difference which is clearly evident in comparing Fig. 2A of the present application with Fig. 5G of the Ono reference is now clearly defined in both of the independent claims 1 and 2. Specifically, in Fig. 5G of Ono, the gate insulating film 111 is formed so that its upper and lower edges are both essentially in the same location relative to the edges of the gate electrode 106. In

Fig. 2A of the present application, on the other hand, it is clear that the upper end portions of the gate insulating film 103 are inward relative to both the end portions of the gate electrodes 104 and the lower end portions of the gate insulating film 106. This structure creates the gradual decreasing thickness for the high dielectric constant gate insulating film 103 which creates the benefits of reduced metal introduction into the underlying source and drain regions and reduced fringe capacitance. No such advantage will be achieved in the gate insulating structure of the Ono device.

Reconsideration and allowance of amended claim 4 over the 35 U.S.C. § 103 rejection based on Ono and Abrokwah (USP 5,514,891) is also respectfully requested. Although Abrokwah is of general interest with regard to providing an undercut t-shaped gate structure, as noted in the Office Action, absolutely nothing in Abrokwah teaches or suggests the formation of the high dielectric constant insulating film to have the structure discussed above with the upper end portion of the gate insulating film located inwardly of both the end portions of the gate electrode and the lower end portions for the gate insulating film itself. Therefore, again, nothing would suggested the tapered arrangement of the gate insulating film 103 shown in Fig. 2A and defined by claim 4 with the gradually decreasing thickness for the high dielectric constant gate insulating film which leads to the advantages of the present invention. Accordingly, reconsideration and allowance of claim 4 over this combination of references is also respectfully requested.

Similarly, reconsideration and allowance of the dependent claims 3, 5 and 7 and newly present claims 21-35 over the cited references is also respectfully requested for reasons set forth below.

With regard to new dependent claims 21 and 22, these claims define that the lower end portions of the gate insulating film are formed outwardly of the end portions of the gate electrodes, as clearly shown in Fig. 2A. This is completely different from the structure of either Ono or Abrokwah since, in both cases, both the upper and lower end portions of the gate insulating film are formed inwardly of the overlapping gate electrode structure.

New independent claim 23 defines the features of the invention in terms of means for reducing an amount of metal introduced into a silicon substrate from the metal gate insulating film. Absolutely nothing in either Ono or Abrokwah suggests the claimed means for reducing the introduction of metal based on forming the upper end portions of the gate insulating film inwardly of the end parts of the gate electrode and reducing the thickness of the gate insulating film in areas in which the gate electrode extends over the source and drain regions. The dependent claims 23-28 further define the structural differences including the reduction of the thickness of the gate insulating film in a tapered manner between the upper end portions and the lower end portion (claim 24). In addition, claim 27 specifically defines the formation of a second gate insulating film having a lower dielectric constant than the gate insulating film in the areas of the gate insulating film under the gate electrode and between the upper end portions and lower end portions of the gate insulating film. As such, claim 27 defines the feature of the low dielectric constant insulating film such as 106 shown in Fig. 2A. New independent claim 29 combines features of claims 20-24, 25, 26, and 27 into a single independent claim having all of the distinctions over the prior art discussed above.

In addition, new independent claim 33 and its dependent claims 34 and 35 define features of the invention in terms of means for reducing fringe capacitance in

areas where the gate electrode overlaps the source and drain regions. Again, absolutely nothing in the cited prior art suggests such a means to reduce fringe capacitance based on the location of the upper end portions of the gate insulating film inwardly from the end portions of the gate electrode.

Accordingly, for the reasons set forth above, reconsideration and allowance of claims 1-5, 7 and 21-35 is earnestly solicited.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of either by telephone discussion or by personal interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 01-2135 (Case No. 520.40885X00), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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APPENDIX A

Attached Material

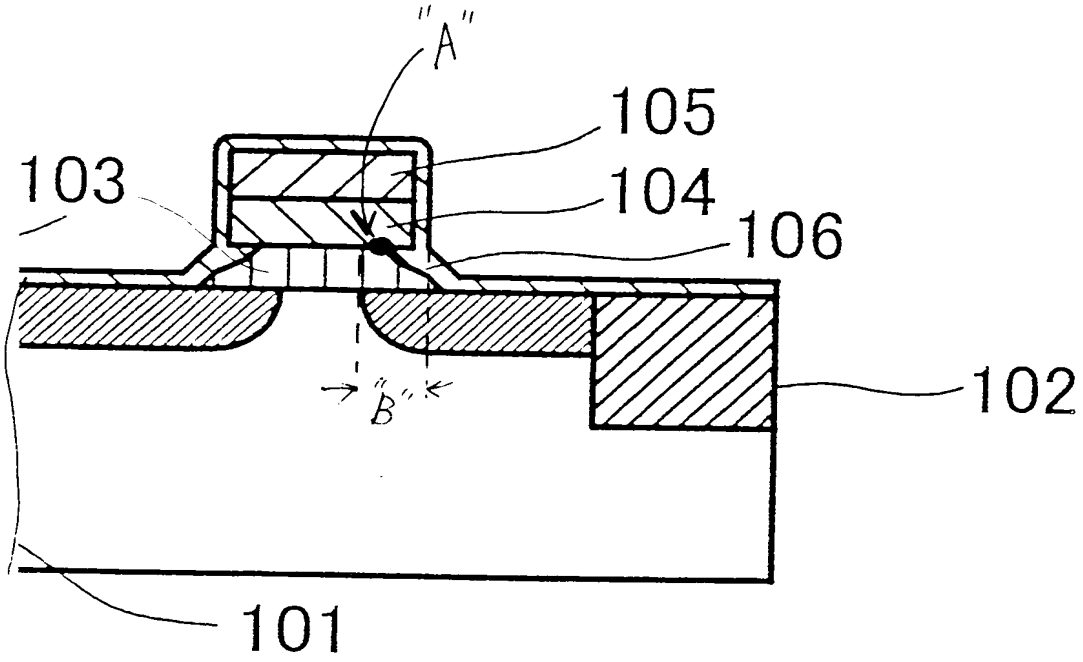

Fig. 1 (the same figure with FIG. 2A of the present specification)

APPENDIX B

FIG. 2A

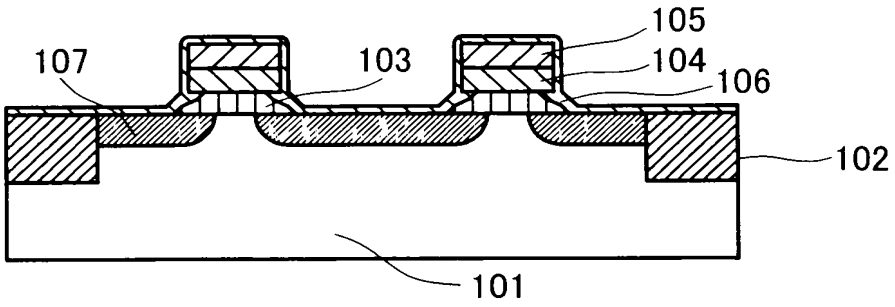

FIG. 2B

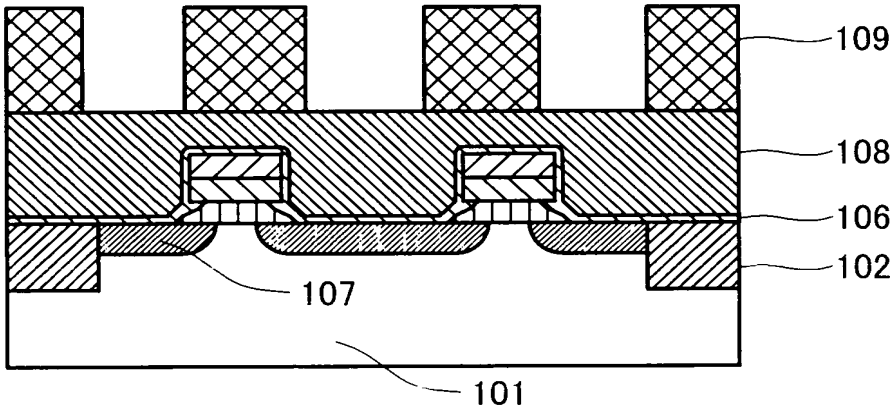

FIG. 2C